

## CLAIMS

What is claimed is:

1        1. A method for chemical vapor deposition or atomic  
2 layer deposition of aluminum oxide comprising:

3  
4        (a) providing an aluminum alkoxide precursor that is  
5 dissolved, emulsified or suspended in a liquid;

6  
7        (b) providing a vapor generated from the aluminum  
8 alkoxide precursor; and

9  
10       (c) depositing an aluminum oxide film from said vaporized  
11 precursor on a substrate at a temperature greater than  
12 500°C.

1       2. The method of claim 1 wherein an oxidizing reactant  
2 is introduced separately from said vaporized aluminum  
3 alkoxide.

1       3. The method of claim 2 wherein said oxidizing reactant  
2 is selected from the group consisting of oxygen, ozone,  
3 water, hydrogen peroxide, nitrous oxide, and combinations  
4 thereof.

1       4. The method of claim 1 wherein the aluminum alkoxide  
2 precursor includes aluminum alkoxide selected from the  
3 group consisting of aluminum iso-propoxide, aluminum  
4 sec-butoxide, aluminum ethoxide, aluminum neo-pentoxide,  
5 aluminum iso-butoxide, aluminum methoxide, aluminum

6 propoxide, aluminum butoxide, aluminum tertiary-butoxide,  
7 and aluminum phenoxide.

1 5. The method of claim 1 wherein the liquid is selected  
2 from the group consisting of pentane, hexane, octane,  
3 heptane, nonane, decane, dodecane, iso-propanol,  
4 tetrahydrofuran, and butyl acetate.

1 6. The method of claim 1 wherein the liquid is selected  
2 from the group consisting aliphatic hydrocarbons,  
3 aromatic hydrocarbons, alcohols, ethers, aldehydes,  
4 ketones, acids, phenols, esters, amines, alkyl nitriles,  
5 halogenated hydrocarbons, silylated hydrocarbons,  
6 thioethers, amines, cyanates, isocyanates, thiocyanates,  
7 silicone oils, nitroalkyls, alkyl nitrates and/or mixtures  
8 of one or more of the above.

1 7. The method of claim 1 wherein the aluminum alkoxide  
2 of said precursor is aluminum iso-propoxide and the  
3 liquid is iso-propanol.

1 8. The method of claim 1 wherein the aluminum alkoxide  
2 of said precursor is aluminum iso-propoxide and the  
3 liquid is octane.

1 9. The method of claim 1, wherein the vapor of the  
2 aluminum alkoxide precursor is obtained from the  
3 vaporization of a mixture of aluminum alkoxide and a  
4 liquid wherein the liquid vaporizes at a higher  
5 temperature than the aluminum alkoxide such that the  
6 liquid is not vaporized when the aluminum alkoxide is

7 vaporized and the nonvaporized liquid is diverted from  
8 the chemical vapor deposition reactor.

1 10. The method of claim 1 further comprising introducing  
2 the vaporized aluminum alkoxide into a reactor with  
3 separate addition of an oxidant and an inert purge gas  
4 and depositing a film on said substrate by sequential  
5 introduction of alternating pulses of vaporized aluminum  
6 alkoxide(s), purge gas, co-reactant(s) and purge gas.

1 11. The method of claim 1 wherein the substrate is  
2 selected from the group consisting of semiconductor  
3 substrates, dielectrics, metals, organic substrates,  
4 glasses, metal oxides, and plastic polymeric substrates,  
5 Si-containing semiconductor substrates, silicon on  
6 insulator substrates, Si substrates, Ge substrates, SiGe  
7 substrates, GaAs substrates, InP substrates and mixtures  
8 or multilayers thereof.

1 12. A multilayer structure incorporating aluminum oxide  
2 deposited according to claim 1.

1 13. A multicomponent film incorporating aluminum oxide  
1 deposited according to claim 1.

1 14. An electronic device that contains aluminum oxide  
2 deposited according to claim 1.

1 15. The electronic device of claim 14 selected from the  
2 group consisting of a transistor, capacitor, diode,  
3 resistor, switch, light emitting diode, laser, wiring  
4 structure, and interconnect.

1 16. A capacitor structure fabricated by sequentially  
2 depositing a bottom electrode layer, a dielectric layer  
3 and a top electrode layer on a base structure wherein the  
4 dielectric layer incorporates aluminum oxide deposited  
5 according to claim 1.

1 17. The capacitor structure of claim 16 wherein the  
2 capacitor structure is selected from the group consisting  
3 of stack capacitors and trench capacitors.

1 18. The capacitor structure of claim 16 further  
2 comprising depositing a dielectric buffer layer over the  
3 capacitor structure.

1 19. The capacitor structure of claim 18 wherein the  
2 optional dielectric buffer layer is selected from the  
3 group consisting of aluminum oxide and a multilayer  
4 structure with aluminum oxide and any insulating material  
5 wherein aluminum oxide is deposited according to claim 1.

1 20. The capacitor structure of claim 16 wherein the  
2 capacitor structure is connected to underlying circuitry  
3 via a plug and optional barrier.

1 21. The capacitor structure of claim 20 wherein the plug  
2 material is selected from the group consisting of  
3 polysilicon, W, Mo, Ti, Cr, Cu, and doped or undoped  
4 alloys, mixtures or multilayers thereof.

1 22. The structure of claim 20 wherein the conductive  
2 barrier is selected from the group consisting of TaN,

3 TaSiN, TiAlN, TiSiN, TaSiN, TaWN, TiWN, TaSiN, TaAlN,  
4 NbN, ZrN, TaTiN, TiSiN, TiAlN, IrO<sub>2</sub>, SiC, TiPt, TiNPt,  
5 TiAlN-Pt, Ru, RuO<sub>2</sub>, RuPt, RuO<sub>2</sub>, WSi, Ti, TiSi, doped and  
6 undoped polysilicon, Al, Pd, Ir, IrO<sub>x</sub>, Os, OsO<sub>x</sub>, MoSi,  
7 TiSi, ReO<sub>2</sub>, and doped or undoped alloys, mixtures or  
8 multilayers thereof.

1 23. The structure of claim 16 wherein the bottom  
2 electrode is selected from the group consisting of  
3 conductive materials, polysilicon, Ni, Pd, Pt, Cu, Ag,  
4 Au, Ru, Ir, Rh, IrO<sub>x</sub>, RuO<sub>x</sub>, TaN, TaSiN, Ta, SrRuO<sub>3</sub>,  
5 LaSrCoO<sub>3</sub>, and doped or undoped alloys, mixtures or  
6 multilayers, thereof.

1 24. The structure of claim 16 wherein the dielectric  
2 material is selected from the group consisting of  
3 aluminum oxide and a multilayer structure of aluminum  
4 oxide and any insulating material.

1 25. The structure of claim 16 wherein the top electrode  
2 is selected from the group consisting of polysilicon, Ni,  
3 Pd, Pt, Cu, Ag, Au, Ru, Ir, Rh, IrO<sub>x</sub>, RuO<sub>x</sub>, TaN, TaSiN, Ta,  
4 SrRuO<sub>3</sub>, LaSrCoO<sub>3</sub>, and doped or undoped alloys, mixtures or  
5 multilayers thereof.

1 26. A wiring structure formed by etching trenches and  
2 vias into a dielectric layer, patterning the  
3 metallization layer, depositing an optional barrier  
4 material, and depositing a wiring material, wherein the  
5 dielectric layer and/or the optional barrier material  
6 incorporate aluminum oxide deposited according to claim  
7 1.

1 27. The structure of claim 26 wherein the dielectric  
2 layer is selected from the group consisting of aluminum  
3 oxide and multilayers of aluminum oxide and  $\text{SiO}_2$ ,  $\text{SiO}_x\text{N}_y$ ,  
4  $\text{Si}_3\text{N}_4$ , phosphosilicate glass, metal oxides, doped or  
5 undoped alloys, mixtures or multilayers, thereof, wherein  
6 aluminum oxide is deposited according to claim 1.

1 28. The structure of claim 26 wherein the optional  
2 barrier material is selected from the group consisting of  
3 aluminum oxide and doped or undoped alloys, mixtures or  
4 multilayers, thereof of aluminum oxide and WN, TiN, TaN,  
5  $\text{SiO}_2$ ,  $\text{SiO}_x\text{N}_y$ ,  $\text{Si}_3\text{N}_4$ , phosphosilicate glass, metal oxides,  
6 wherein aluminum oxide is deposited according to claim 1.

1 29. The structure of claim 26 wherein the wiring  
2 material is selected from the group consisting of  
3 polysilicon, Al, W, Mo, Ti, Cr, Cu and doped or undoped  
4 alloys, mixtures or multilayers thereof.

1 30. A structure comprising a substrate having source and  
2 drain regions and a channel region between said source  
3 and drain regions; depositing a gate dielectric, aligned  
4 to and on top of said channel region; and depositing a  
5 gate electrode aligned to and on top of said gate  
6 dielectric wherein the gate dielectric incorporates  
7 aluminum oxide deposited according to claim 1.

1 31. A method of fabricating an electronic device  
2 comprising: providing a silicon substrate having a first  
3 region doped with a first dopant type and a second region  
4 doped with a second dopant type; forming a gate

5 dielectric layer on said substrate; forming a mold layer  
6 on said gate dielectric; forming a first trench in said  
7 mold layer; forming a first liner in said trench, said  
8 first liner comprised of an alloy having a first work  
9 function; filling said trench with a gate conductor to  
10 form a first gate; forming a second trench in said mold  
11 layer; forming a second liner in said trench, said first  
12 second comprised of an alloy having a second work  
13 function; filling said trench with a gate conductor to  
14 form a second gate; ion implanting a first dopant type on  
15 either side of said second gate to form source drain  
16 regions in said substrate; and ion implanting a second  
17 dopant type on either side of said first gate to form  
18 source drain regions in said substrate wherein the gate  
19 dielectric incorporates aluminum oxide deposited  
20 according to claim 1.

1 32. The structure of claim 30 wherein the gate  
2 dielectric selected from the group consisting of aluminum  
3 oxide and doped or undoped alloys, mixtures or  
4 multilayers of aluminum oxide and  $\text{SiO}_2$ ,  $\text{SiO}_x\text{N}_y$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{BaO}$ ,  
5  $\text{SrO}$ ,  $\text{CaO}$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{La}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ , yttrium  
6 aluminate, lanthanum aluminate, lanthanum silicate, yttrium  
7 silicate, hafnium silicate, zirconium silicate, wherein  
8 aluminum oxide is deposited according to claim 1.

1 33. The structure of claim 30 wherein the gate  
2 dielectric is composed of more than one layer and at  
3 least one component of at least one of the layers  
4 comprising the gate dielectric is aluminum oxide  
5 deposited according to claim 1.

1 34. The structure of claim 30 wherein the multilayer  
2 gate dielectric is composed of a lower, middle and  
3 optional upper layer wherein at least one layer or one  
4 component of a layer of the gate dielectric is aluminum  
5 oxide deposited according to claim 1.

1 35. The structure of claim 34 wherein the lower layer is  
2 selected from the group consisting of  $\text{SiO}_2$ ,  $\text{SiO}_x\text{N}_y$ ,  $\text{Si}_3\text{N}_4$ ,  
3  $\text{BaO}$ ,  $\text{SrO}$ ,  $\text{CaO}$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{La}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ ,  
4 yttrium aluminate, lanthanum aluminate, lanthanum silicate,  
5 yttrium silicate, hafnium silicate, zirconium silicate,  
6 and doped or undoped alloys, mixtures or multilayers,  
7 thereof.

1 36. The structure of claim 34 wherein the middle layer  
2 is selected from the group consisting of  $\text{SiO}_2$ ,  $\text{SiO}_x\text{N}_y$ ,  
3  $\text{BaO}$ ,  $\text{SrO}$ ,  $\text{CaO}$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{La}_2\text{O}_3$ ,  
4  $\text{Y}_2\text{O}_3$ , yttrium aluminate, lanthanum aluminate, lanthanum  
5 silicate, yttrium silicate, hafnium silicate, zirconium  
6 silicate, and doped or undoped alloys, mixtures or  
7 multilayers, thereof.

1 37. The structure of claim 34 wherein the upper layer is  
2 selected from the group consisting of  $\text{SiO}_2$ ,  $\text{SiO}_x\text{N}_y$ ,  $\text{Si}_3\text{N}_4$ ,  
3  $\text{BaO}$ ,  $\text{SrO}$ ,  $\text{CaO}$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{La}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$ ,  
4 yttrium aluminate, lanthanum aluminate, lanthanum silicate,  
5 yttrium silicate, hafnium silicate, zirconium silicate,  
6 and doped or undoped alloys, mixtures or multilayers,  
7 thereof.

1 38. The structure of claim 30 wherein the gate electrode  
2 is selected from the group consisting of polysilicon, Al,



3 Ag, Bi, Cd, Fe, Ga, Hf, In, Mn, Nb, Y, Zr, Ni, Pt, Be,  
4 Ir, Te, Re, Rh, W, Mo, Cr, Fe, Pd, Au, Rh, Ti, Cr, Cu,  
5 and doped or undoped alloys, mixtures or multilayers,  
6 thereof.